Yan Peng

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Research Interest

Formal verification, SAT/SMT solvers, Theorem Proving, Model Checking

Education

University of British Columbia — Vancouver, Canada
Ph.D. Candidate in Computer Science, GPA: 92.5% — 2015–Now

- Supervisor: Mark R. Greenstreet
- Thesis Title: Reflection-based Integration of SMT Solvers into Theorem Provers

University of British Columbia — Vancouver, Canada
M.Sc. in Computer Science, GPA: 92.5% — 2012–2015

- Supervisor: Mark R. Greenstreet
- Thesis Title: Combining SMT with theorem proving for AMS verification : analytically verifying global convergence of a digital PLL

Zhejiang University — Hangzhou, China
B.Eng. in Computer Science and Technology, GPA: 3.87/4.00 — 2008–2012

- Advisor: Jian Shao
- Thesis: Research on Technology of Large-Scale Web Video Topic Discovery

Chu Kochen Honors College — Hangzhou, China
English Minor in Foreign Languages and Engineering Platform — 2008–2012

Experience

University of British Columbia — Vancouver, Canada
Research Assistant at Formal Methods Lab — 2012–now

- **Smtlink**: an Integration of SMT Solvers into the Theorem Prover ACL2
  - The integration contains **verified β-reduction and type inference**
  - It supports rich datatypes including algebraic datatypes and abstract type
- Verifying Safety Properties of an Asynchronous Pipeline Using Smtlink
  - Used **timed traces** to model timed asynchronous circuits with **nondeterminism**
  - Verified **hazard-freedom** and **deadlock-freedom** of an asynchronous pipeline
- Verifying Global Convergence (a Liveness Property) of a Phase-Locked Loop Using Smtlink
  - Built a recurrence relation model and proved convergence using **progress arguments** and **induction**
- Machine Learning Related: Proved the Cauchy-Schwarz Inequality using Smtlink

Oracle — Redwood Shores, US
Student Intern at Oracle Labs — Multiple times since 2014

- Detecting Synthesis-generated Glitches Using SAT Solving and Theorem Proving
  - Formally defined synthesis-generated glitch using three-valued logic
  - Built **Glitch Hunter** using theorem prover ACL2 and SAT solver Glucose that **automatically** detects glitch errors in clock domain crossing logic
  - Built a **Parallel Glitch Hunter** to solve large industrial designs, and successfully found glitch errors in industrial designs

Publications

1. **Type Inference Using Meta-extract for Smtlink and Beyond**, **Yan Peng** and Mark R. Greenstreet, *the Sixteenth International Workshop on the ACL2 Theorem Prover and its Applications (ACL2-2020)*, 2020.
2. **Cauchy-Schwarz in ACL2(r) Abstract Vector Spaces**, Carl Kwan, **Yan Peng** and Mark R. Greenstreet, *the Sixteenth International Workshop on the ACL2 Theorem Prover and its Applications (ACL2-2020)*, 2020.
3. **Verifying Timed, Asynchronous Circuits Using ACL2**, **Yan Peng** and Mark R. Greenstreet, *2019 25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC-2019)*, 2019.
4. **Smtlink 2.0**, **Yan Peng** and Mark R. Greenstreet, *the Fifteenth International Workshop on the ACL2 Theorem Prover and its Applications (ACL2-2018)*, 2018.
5. **Defining and Detecting Synthesis-generated Glitches**, **Yan Peng**, Mark R. Greenstreet, Ian W. Jones, *the 56th Design Automation Conference (DAC-2018)*, 2018. (poster)
6. **Finding Glitches Using Formal Methods**, **Yan Peng**, Ian W. Jones, and Mark R. Greenstreet, *2016 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC-2016)*, 2016.
7. **Extending ACL2 with SMT Solvers**, **Yan Peng** and Mark R. Greenstreet, *the Thirteenth International Workshop on the ACL2 Theorem Prover and its Applications (ACL2-2015)*, 2015.
8. **Integrating SMT with Theorem Proving for Analog/Mixed-Signal Circuit Verification**, **Yan Peng** and Mark R. Greenstreet, *the Seventh NASA Formal Methods Symposium (NFM-2015)*, 2015.
9. **Verifying Global Convergence for a Digital Phase-Locked Loop**, Jijie Wei, **Yan Peng**, Grace Yu and Mark R. Greenstreet, *2013 Formal Methods in Computer-Aided Design (FMCAD-2013)*, 2013.
10. **Verifying Global Convergence of a Digital Phase-Locked Loop with Z3**, **Yan Peng** and Mark R. Greenstreet, *the International Workshop on Design Automation for Analog and Mixed-Signal Circuits*, 2013. (poster)

Talks

- **Hardware Verification Using Theorem Proving and SMT/SAT Solving**, *IBM, Austin, US, 2018.*
- **Verifying Global Convergence of a Digital Phase-Locked Loop with Z3**, *Microsoft, Redmond, US, 2013.*

Academic Activities

- Reviewer for International Conference on Computer-Aided Verification (CAV-2018)
- Program Committee for 24th International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2-2020)

Teaching

- **Teaching Assistant** at University of British Columbia:

CPSC418 Parallel Computing	2018 W1
CPSC311 Definition of Programming Languages	2015 W1
CPSC312 Functional and Logic Programming	2013 W1
APSC160 Introduction to Computation and Engineering Design	2012 W1

Skills

- **Formal Methods:** Z3, ACL2
- **Programming:** Python, Matlab, Haskell, Erlang, C/C++, Java, Racket, SQL, Bash, CUDA, Prolog, Verilog
- **Tools:** Emacs, LaTeX, Git