ABSTRACT

IC technology continues to closely follow Moore's Law, while the ability to verify designs lags behind. The International Technology Roadmap for Semiconductors (ITRS) predicts production of chips using 16nm technology already by 2015, but the verification gap, i.e., advancements in verification technology not keeping up with advancements in design technology, seems to be also increasing at a fast pace. A recent study shows a drop of nine percentage points in the number of 1st-silicon success from 2002 through 2010. By 2007, more than 2/3 of chips had to be respun due to bugs. The increasing verification gap is to blame. Unfortunately, because more bugs are slipping into the fabricated chip, post-silicon debug is the only way to catch them.

Post-silicon debug is the problem of determining what's wrong when the fabricated chip of a new design behaves incorrectly. The focus of post-silicon debug is *design errors*, whereas traditional VLSI test focuses on random manufacturing *defects* on each fabricated chip. Post-silicon debug currently consumes more than half of the total verification schedule on typical large designs, and the problem is growing worse.

The general problem of post-silicon debug is broad and multi-faceted, spurring a diverse variety of research. In this thesis, I focus on one of the most fundamental tasks: getting an execution trace of on-chip signals for many cycles leading up to an observed bug or crash. Until such a trace is obtained, further debugging is essentially impossible, as there is no way to know what happened on the chip. However, the ever-increasing chip complexity compounded with new features that add non-determinism makes computing accurate traces extremely difficult. Thus, to address this issue, I present a novel post-silicon debug framework, which I call BackSpace. From theory to practice, I have methodically developed this framework showing that BackSpace effectively computes accurate traces leading up to a crash state, has low cost (*zero*-additional hardware overhead), and handles non-determinism. To support my claims, I demonstrated BackSpace with several industrial designs using simulation models, hardware prototypes, and on actual silicon.

BIOGRAPHICAL NOTES

Academic Studies:	M. Sc. in Computer Science, UBC, Canada, 2007 M. Sc. in Electrical Engineering, UFMG, Brazil, 1999 B. Sc. In Electrical Engineering, UFMG, Brazil, 1996
Current Position:	Ph. D. candidate, UBC
Past Positions:	2000-2004 Sr. ASIC Verification Engineer at Mindspeed Tech., Inc. 1998 -2000 ASIC Design Engineer at Smar Research Corporation.

GRADUATE STUDIES

Field of Study: Formal Methods

Courses

		Instructors
CPSC 503	Computational Linguistics I	Dr. Giuseppe Carenini
CPSC 506	Complexity of Computation	Dr. Anne Condon
CPSC 513	Integrated Systems Design	Dr. Alan J. Hu
CPSC 508	Operating Systems	Dr. Charles Krasic
EECE 583	CAD Algorithms for Integrated Circuits	Dr. Steve Wilton
CPSC 421	Introduction to Theory of Computing	Dr. Mark Greenstreet
CPSC 507	Software Engineering	Dr. Gail Murphy
CPSC 538E	Topics in Computer Systems: Computer Architecture	Dr. Mark Greenstreet

RESEARCH INTERNSHIPS

IBM Corporation, Haifa Research Labs, Israel. FALL 2009
This internship included investigating, proposing and developing a new technique for post-Silicon debug. The TAB-BackSpace technique was one of the results of this internship.

Intel Corporation, Oregon, USA. SUMMER 2009
This internship included industrializing a parallel and distributed explicit model checker tool that Brad Bingham and I developed for the CPSC538E course. Our tool, called PReach, was able to verify the largest model yet using explicit state model checking techniques inside Intel at that time. PReach is now being used by other universities and companies.

SELECTED PUBLICATIONS

nuTAB-BackSpace: Rewriting to Normalize Non-Determinism in Post-Silicon Debug Traces, Flavio M. de Paula, Alan J. Hu, Amir Nahir. *To appear* at Computer Aided Verification (CAV'12), USA.

TAB-BackSpace: Unlimited-length Trace Buffers with Zero Additional On-Chip Overhead. Flavio M. de Paula, Amir Nahir, Ziv Nevo, Avigail Orni, Alan J. Hu. Design Automation Conference (DAC'11), USA.

Industrial Strength Explicit State Model Checking. Brad Bingham, Jesse Bingham, Flavio M. de Paula, John Erickson, Gaurav Singh, Mark Reitblatt. Intl. Workshop on Parallel and Distributed Methods in Verification (PDMC'10), The Netherlands.

BackSpace: Moving Towards Reality. Flavio M. de Paula, Marcel Gort, Alan J. Hu, Steve Wilton. Microprocessor Test and Verification (MTV'08), USA.

BackSpace: Formal Analysis for Post-Silicon Debug. Flavio M. de Paula, Marcel Gort, Alan J. Hu, Steve Wilton, Jin Yang. Formal Methods in Computer Aided Design (FMCAD'08), USA.

An Effective Guidance Strategy for Abstraction-Guided Simulation. Flavio M. de Paula, Alan J. Hu. Design Automation Conference (DAC'07), USA.

PRESENTATIONS

BackSpace: Formal Analysis for Post-Silicon Debug. August 10th, 2011, Advanced Micro Devices (AMD), Boxborough, MA.

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Faculty of Graduate Studies

THE UNIVERSITY OF BRITISH COLUMBIA

PROGRAMME

The Final Oral Examination
For the Degree of

DOCTOR OF PHILOSOPHY
(Computer Science)

FLAVIO M. DE PAULA

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Friday, April 27, 2012, 12:30 pm
The Centre for Teaching, Learning & Technology,
University Services Building (2329 West Mall)

"BackSpace: Formal Analysis for Post-Silicon Debug"

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