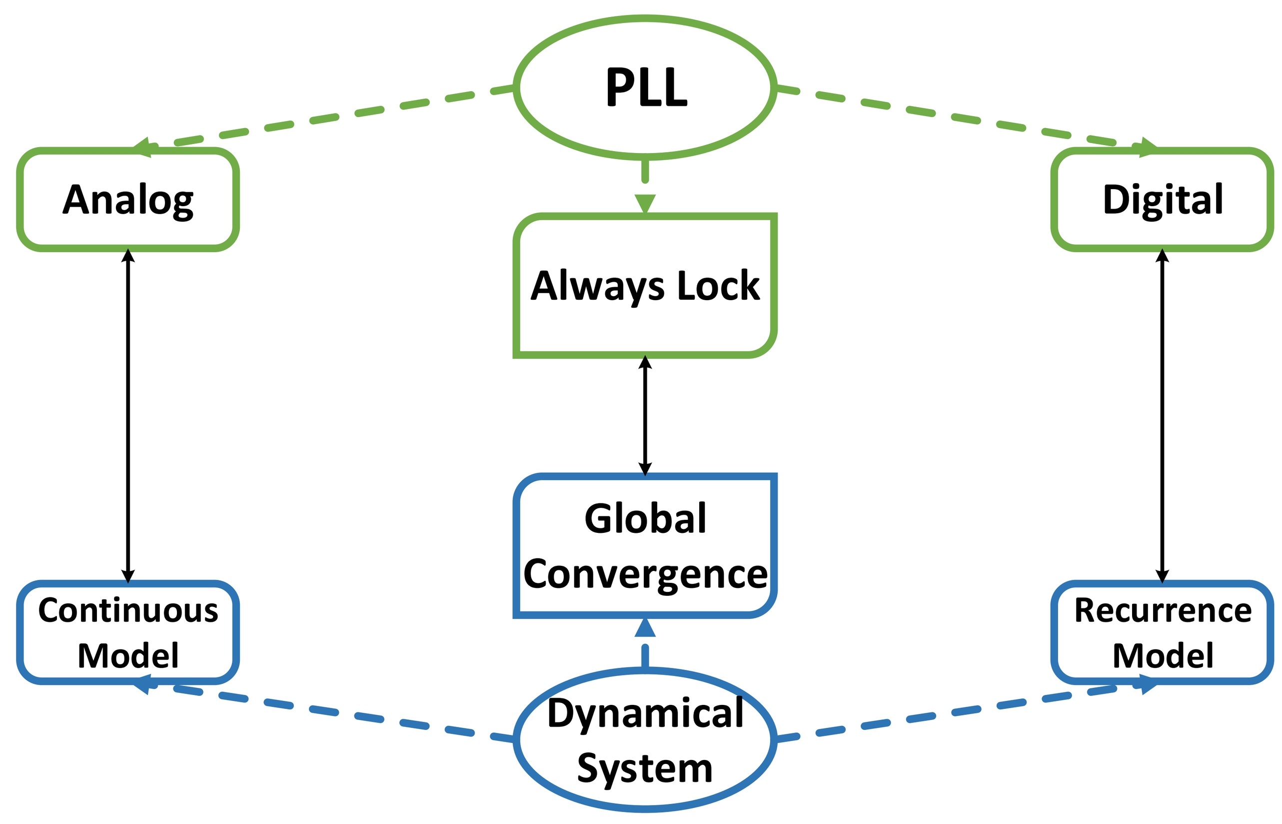
Verifying Global Convergence of a Digital Phase-Locked Loop with Z3

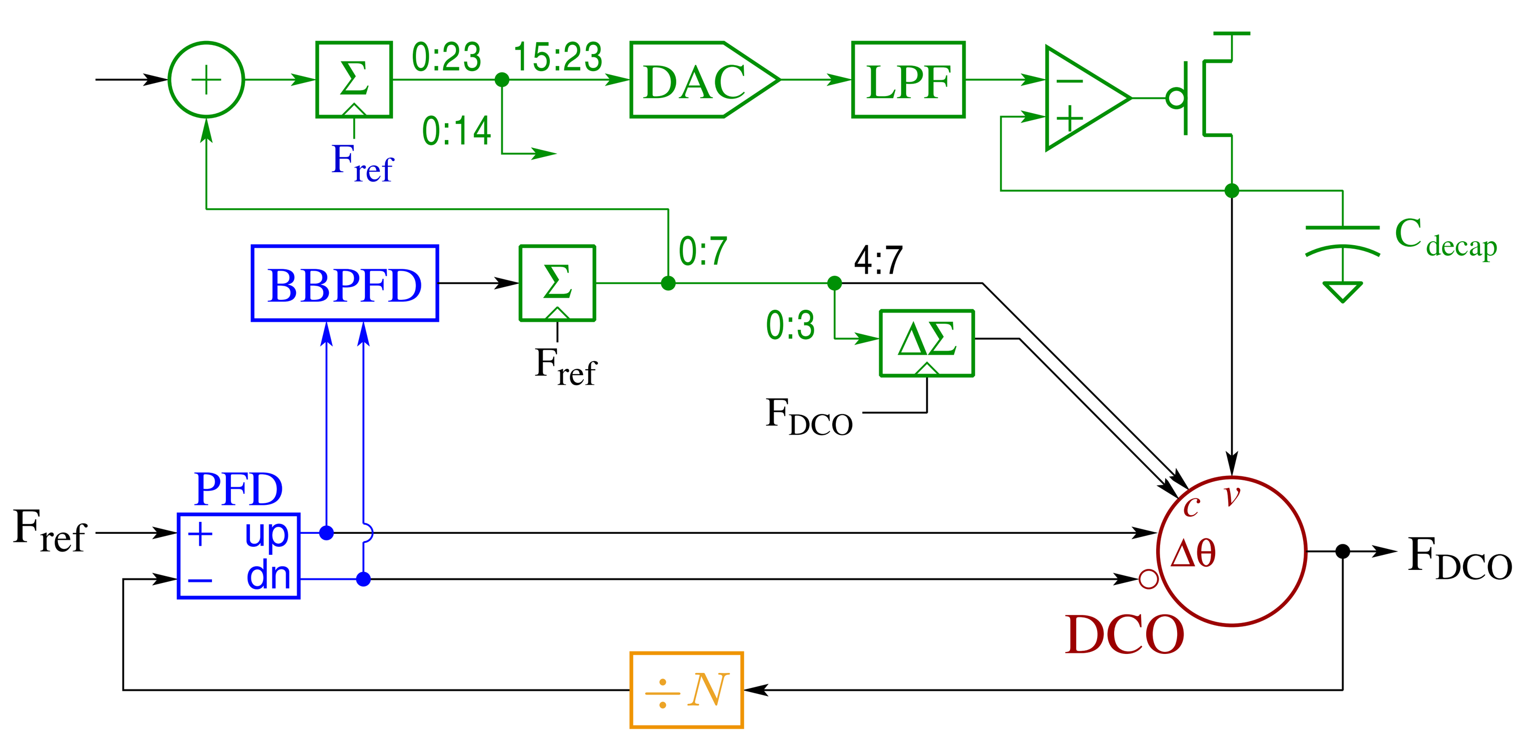
Yan Peng, Mark Greenstreet
University of British Columbia, Canada
{yanpeng, mrg}@cs.ubc.ca

I. Problem: Global Convergence of a PLL



- Phase-locked loops (PLL) are *ubiquitous* in analog and mixed-signal designs.
- Showing convergence to this locked behaviour is *hard*:
  - A large, continuous state space of possible starting conditions.
  - Simulations of convergence are impractical: time-to-lock is very large compared with the time-scales required for accurate circuit simulation.
  - *Coverage achieved by the simulations is quite small.*

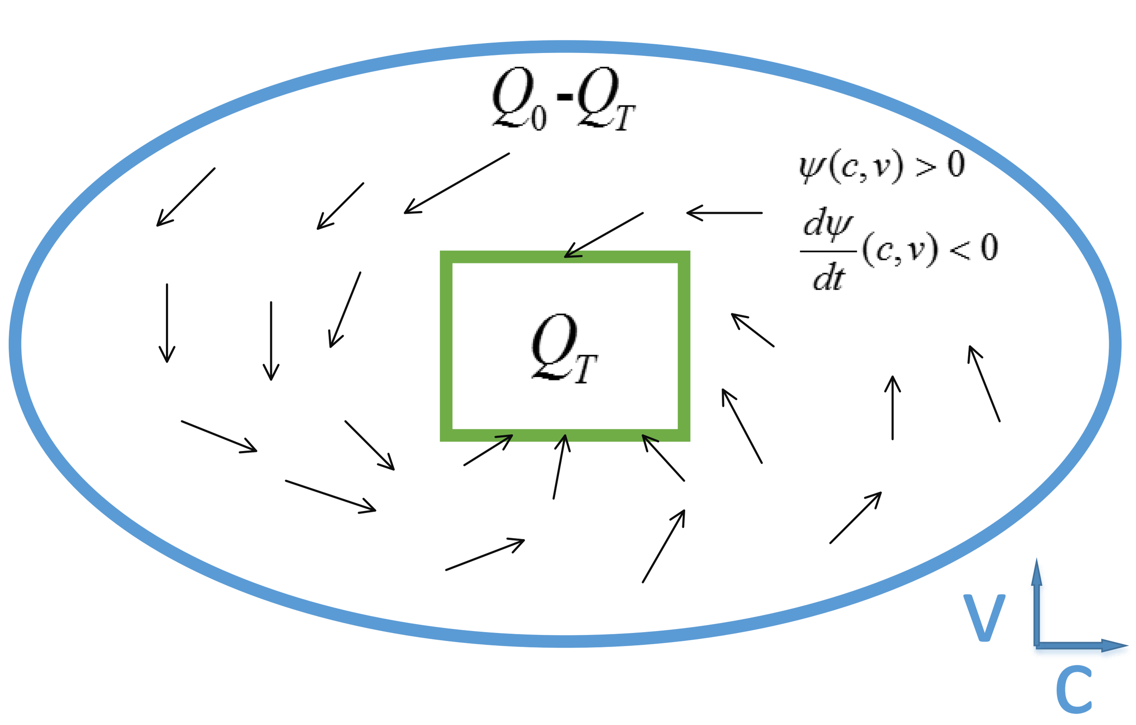
II. A State-of-the-Art Digital PLL (from CICC 2010)



- DCO has three control inputs:
  capacitance setting (digital), supply voltage (linear), phase correction (time-difference of digital transitions).
- Uses linear and bang-bang PFD.
- Integrators are digital.
- LPF and decap to improve power-supply rejection.

III. Lyapunov Function

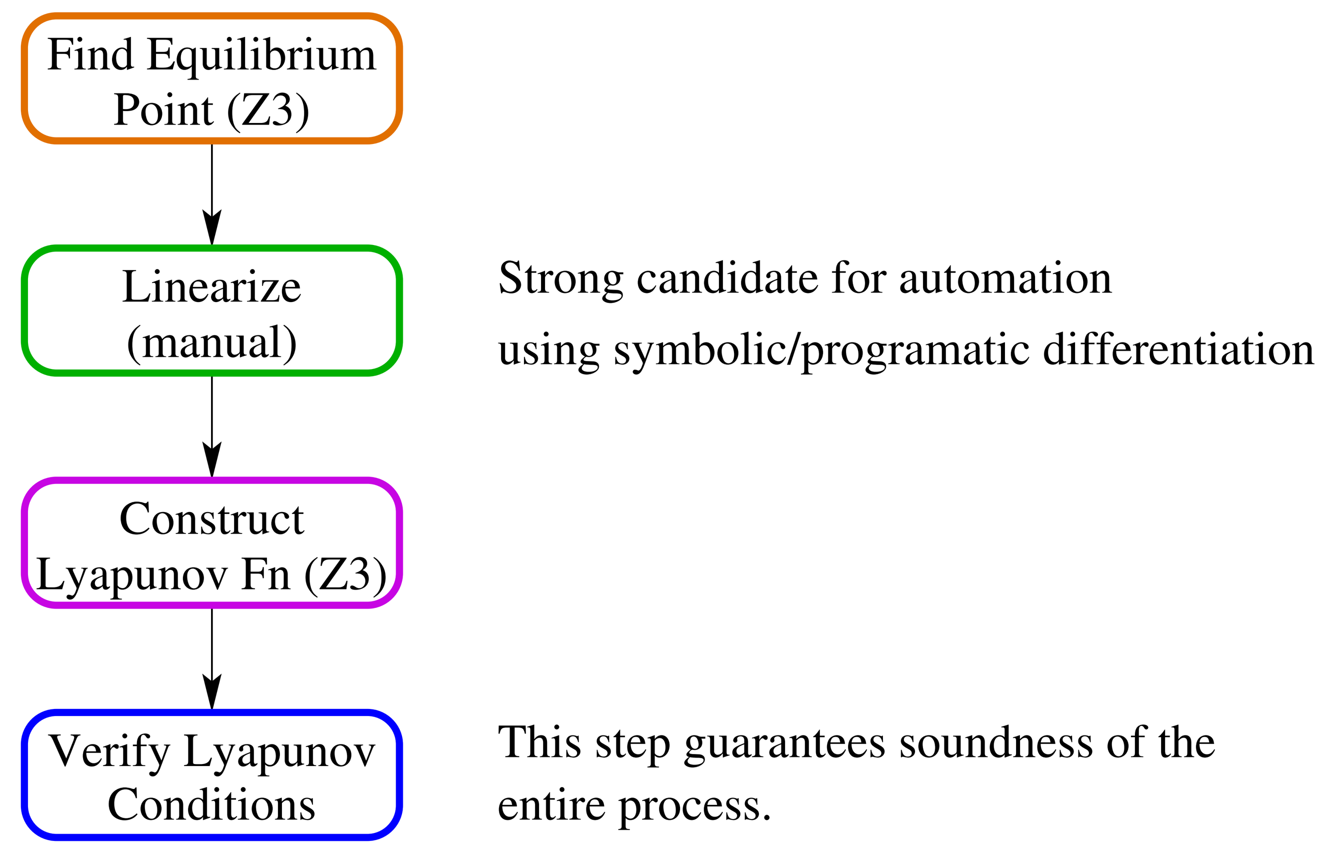
- Continuous counterpart of a ranking function for discrete progress arguments.



IV. Lyapunov Function for Simple Nonlinear ODE

- Linear ODE: $\dot{x} = Ax$
- Let P be the solution of $A^TP + PA = -I$. A possible Lyapunov function becomes $\Psi(x) = X^TPX$.
- If P is positive definite, then the system $\dot{x} = Ax$ globally converges to $x = 0$

V. Verifying a Simplified Nonlinear Model using Z3



- Z3 easily proves global convergence.
- Fixed procedure: promising for automation.

VI. Improve the Model 1

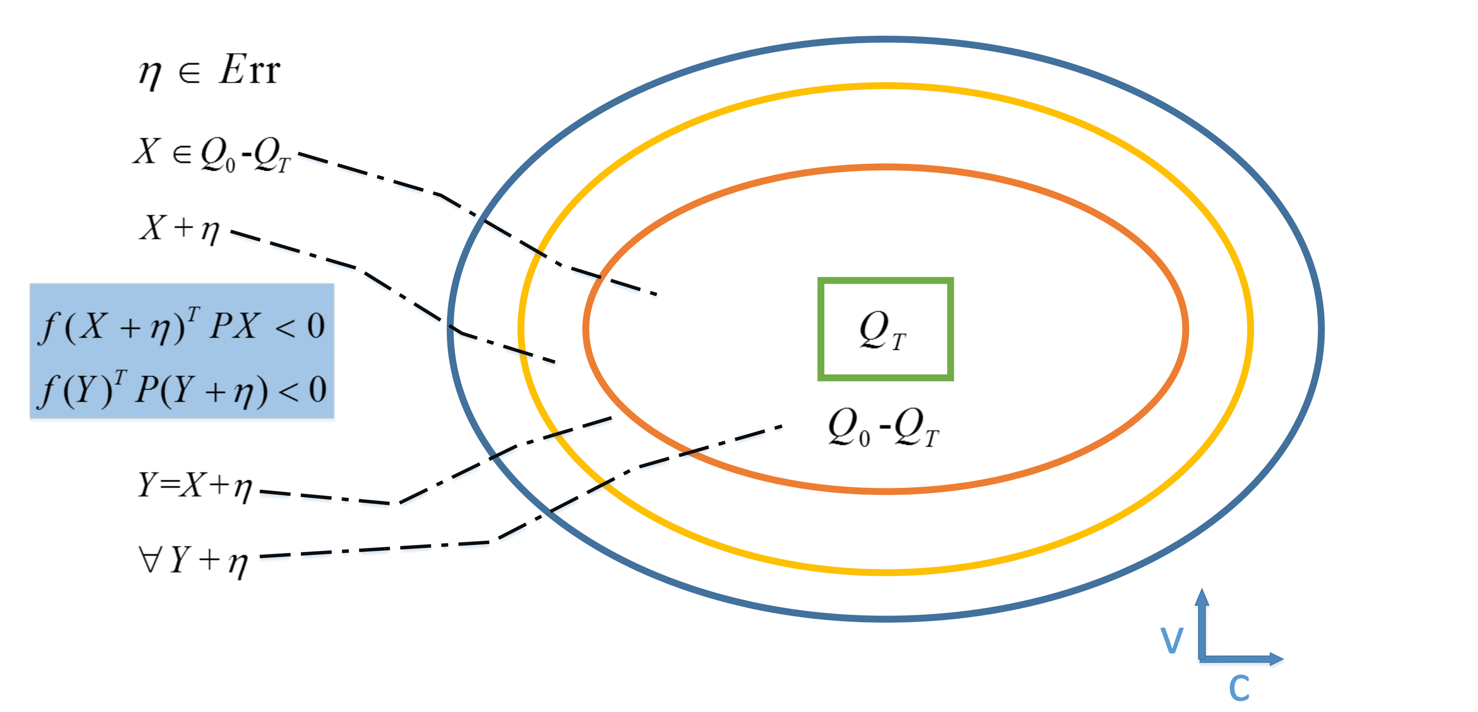
Parameters with ranges:
Inequality ranges for parameters $\alpha \in 1 \pm 0.2$, $\beta \in 1 \pm 0.2$, $v_0 \in 1 \pm 0.2$ and $c_0 \in 1 \pm 0.2$.
Strategy: Check where the parameters are used, try simplify non-linear part.
Example: Simplifying an element of the Jacobian matrix:

$$\frac{g_1 \alpha}{c_0+\beta c_{code}} \rightarrow \frac{g_1}{c_0+\beta c_{code}}$$

The approximation is based on the observation that $\alpha \in 1 \pm 0.2$.

VII. Improve the Model 2

Adding quantization error:
Need to show: $\forall x \in Q_0 - Q_T . \forall \eta \in Err . f(x+\eta)^T P x < 0$, where f is nonlinear. This creates nonlinear terms for the components of η.
Strategy: This is equivalent to: $\forall x \in (Q_0 - Q_T) \oplus Err . \forall \eta \in Err . (x + \eta \in Q_0 - Q_T) \Rightarrow (h(x)^T P (x+\eta) < 0)$



The Minkowski sum of two sets, $A \oplus B$, is the set of elements that can be obtained as the sum of an element from A and an element from B:

$$A \oplus B \quad = \quad \{z \mid \exists a \in A. \exists b \in B. z = a + b\}$$

VIII. Conclusion & Future Work

- Conclusion:
  - Using a simplified model, we showed convergence where specifications for components are interval bounds using Z3.
  - SMT-based methods can address these problems more effectively than traditional simulation techniques.
- Future work:
  - Provide bounds on lock time.
  - Examine other digital PLL architectures to assess the reusability and automatability of this verification.
  - *Component validation:* formalize the connection between the models used and those used in other phases of the analog and mixed-signal design process.