## YAN PENG

#### University Address

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## Contact

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## ABSTRACT

Fourth-year **PhD** candidate looking for job opportunities in applying formal methods including **theorem proving** and **SAT/SMT** solving to *machine learning* problems, *concurrent systems* and *hardware verifica-tion* problems.

#### EDUCATION

Doctor of Philosophy, Computer Science	GPA 92.5 $\%$
University of British Columbia, Vancouver, BC	Expected Nov. 2019
Master of Science, Computer Science	GPA 92.5 %
University of British Columbia, Vancouver, BC THESIS - Combining SMT with Theorem Proving for AMS Verification	Sept. 2015
THESIS - Combining SMT with Theorem Proving for AMS Vernication	
Bachelor of Engineering, Computer Science and Technology	Major GPA 3.9/4.0
Zhejiang University, Hangzhou, Zhejiang	June 2012
THESIS - Research on Technology of Large-Scale Web Video Topic Discovery	
Chu Kashan Hanang Callaga Fansign Languages & Engineering platform	English Minor
Chu Kochen Honors College, Foreign Languages & Engineering platform	English Minor
Zhejiang University, Hangzhou, Zhejiang	June 2012

## **RESEARCH EXPERIENCE**

Research Assistant (Ph.D. Candidate) Integrated System Design Lab, University of British Columbia Aug. 2012 - Now

- **Smtlink**: Combining Theorem Proving with SMT to verify properties of Analog/Mixed-Signal circuits, asynchronous circuits and machine learning algorithms (project link)
  - Built an extensible and sound architecture for integrating Z3 into the ACL2 theorem prover
  - Verified global convergence for a digital PLL using Smtlink
  - Verify safety, liveness and functional correctness properties of asynchronous circuits (ongoing)
- Automatic differentiation: Using automatic differentiation to calculate small signal response and parameter sensitivities of circuits
- **Tool optimization:** Optimizing the internal circuit representation of the Coho reachability analysis tool to improve its simulation performance

Student Intern (Multiple) Oracle Labs, Redwood Shores, CA, US

Aug. 2014 (Full-time)
Nov. 2014 - Dec. 2014 May 2015 - Jan. 2017 (Part-time)
Jan. 2017 - March 2017 (Full-time)
May 2017 - April 2018 (Part-time)
June 2010 - June 2012

Multi-model integration, K-partite graph clustering

## PUBLICATIONS

#### Verifying Timed, Asynchronous Circuits using ACL2 [Full paper]

**Y. Peng**, M. Greenstreet, 25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC-2019).

## Smtlink 2.0 [Full paper]

**Y. Peng**, M. Greenstreet, 15th International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2-2018).

## Defining and Detecting Synthesis-generated Glitches [Poster]

Y. Peng, M. Greenstreet, I. Jones, the 56th Design Automation Conference (DAC-2018).

## Finding Glitches Using Formal Methods [Short paper]

**Y. Peng**, I. Jones, M. Greenstreet, the 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC-2016).

#### Extending ACL2 with SMT Solvers [Full paper]

**Y. Peng**, M. Greenstreet, the 13th Inernational Workshop on the ACL2 Theorem Prover and Its Applications (ACL2-2015).

# Integrating SMT with Theorem Proving for Analog/Mixed-Signal Circuit Verification [Full paper]

Y. Peng, M. Greenstreet, the 7th International NASA Formal Methods Symposium (NFM-2015).

# Combining SMT with Theorem Proving for AMS Verification: Analytically Verifying Global Convergence of a Digital PLL [Thesis]

Master of Science, Computer Science program, University of British Columbia, Vancouver, BC, Canada, April 28th 2015.

#### AMS Verification with Theorem Proving and SMT [Abstract]

Y. Peng, M. Greenstreet, the International Workshop on Frontiers in Analog CAD (FAC-2014).

## Verifying Global Convergence for a Digital Phase-Locked Loop [Full paper]

J. Wei, **Y. Peng**, G. Yu, M. Greenstreet, the 13th Conference on Formal Methods in Computer Aided Design (FMCAD-2013).

## Verifying Global Convergence of a Digital Phase-Locked Loop with Z3 [Poster]

Y. Peng, M. Greenstreet, the International Workshop on Design Automation for Analog and Mixed-Signal Circuits (2013).

<b>TALK</b> Hardware Verification Using Theorem Proving and SMT/SAT Solving IBM, Austin, Texas, US.	Nov. 2018	
Verifying Global Convergence of a Digital Phase-Locked Loop with Z3 Microsoft, Redmond, WA, US.	Sept. 2013	
<b>PEER REVIEWING SERVICE</b> Reviewer of International Conference on Computer-Aided Verification (CAV-2018)		
TEACHING EXPERIENCE		
CPSC418 - Parallel Computing Course description: Parallel computing algorithms and architecture (Erlang and CUDA)	Sept. 2018 - Now	

CPSC311 - Definition of Programming Languages Course description: Programming language theory	Sept. 2015 - Dec. 2015
CPSC312 - Functional and Logic Programming Course description: Functional and logic programming (Haskell and Prolog)	Sept. 2013 - Dec. 2013

APSC160 - Introduction to Computation in Engineering Design Sept. 2012 - Dec. 2012 Course description: C and hardware IO programming

## SELECTED COURSE PROJECTS

Automate Convergence Rate Proof for Gradient Descent on Quadratic Functions Course: CPSC540 - Machine Learning	2014, Winter, 1st Term
Automatic Differentiation and Continuous System Formal Verification Course: CPSC513 - Formal Verification	2013, Winter, 2nd Term

## SKILLS

Research-related Languages/Tools: ACL2, Z3 Experienced: Python, Common Lisp, Erlang, Racket, Haskell, Prolog, CUDA, C, C++, C#, Java, MAT-LAB, bash, SQL, assembly language, Verilog, and SPICE. Others: Emacs, Git,  ${\rm \ensuremath{\mathbb E}T_FX}$ 

## EXTRACURRICULAR ACTIVITIES

Girls Learning Code Intro to Python for Teen Girls (ages 12-17), volunteer June 2016 Microsoft Technology Club, Operation Group, Group leader Sept. 2008 - June 2012 • Microsoft Asia Research Institute Campus Tour, Assistant March 2010 • The Fourth C Language Competition, Project Manager

• MSTC Academic Lecture Series, Project Manager

Dec. 2009 March 2009