

# Celina G. Val

## Contact Information

---

Dept. of Computer Science      Tel: +1 (604) 779-6687  
Univ. of British Columbia      Email: gvcelina@gmail.com  
201-2366 Main Mall  
Vancouver, BC, V6T 1Z4 Canada

## Professional Experience

---

**Software Developer Consultant, Vancouver, Canada**      11/2012 - present

Main Activities:      Developing and optimizing simulation algorithms for Jasper Design Automation.  
Collaborated in the development of a trace visualization tool for Jasper Design Automation.

**Jasper Design Automation, Belo Horizonte, Brazil**      07/2009 - 05/2011

Full-Time R&D Engineer

Main Activities:      Developed efficient hardware modeling and abstraction algorithms applied to a hardware formal verification tool (JasperGold®) using C++.  
Created tests for implemented algorithms using Tcl, Verilog and VHDL.

**Jasper Design Automation, Belo Horizonte, Brazil**      09/2008 - 06/2009

Part-Time Research Intern

Main Activities:      Improved and fixed bugs in VHDL and Verilog compilation modules using Lex and Bison.  
Improved and fixed bugs in circuit modeling inside *JasperGold*®, using C++.

## Technical Skills

---

**Languages**      C/C++, Shell Scripts, Python, Verilog, VHDL, Java, LaTeX

**Softwares**      GNU Make, Gdb, Valgrind, Vim, CVer, JasperGold, Xilinx ISE, NetBeans

## Education

---

**The University of British Columbia, Canada**      09/2011 - present

Master of Science in Computer Science

Thesis Topic:      “Effective Firmware Validation”

Supervisor:      Alan J. Hu

Grade Average:      89.3%

**Federal University of Minas Gerais (UFMG), Brazil**      02/2010 - 08/2011

Master of Science in Computer Science

Thesis Title:      “Dynamic Monitoring of Assertions for Post-Silicon Debug”

Supervisor:      Claudionor José Nunes Coelho Junior

Grade Average:      92.0%

**Federal University of Minas Gerais (UFMG), Brazil**      01/2006 - 08/2009

Bachelor of Science in Computer Science

Grade Average:      86.6%

## Honors and Awards

---

<b>Computer Science Merit Scholarship</b>	Dept. of Computer Science, University of British Columbia, 2011-2013
<b>Second Prize for Best Oral Presentation</b>	X-Meeting - 4 <sup>th</sup> International Conference of The AB3C (Brazilian Association for Bioinformatics and Computational Biology), 2008, for the paper "SIGLa - A Dynamic System to Integrate Laboratory Data Based on Workflow Definition Data" presented by Celina Val

## Research Experience

---

<b>Dept. of Computer Science, The University of British Columbia</b>	09/2011 - Present
Research Assistant at Integrated Systems Design Laboratory	
Main Activities:	Developed a novel symbolic execution algorithm to software verification. Implementing a tool based on KLEE and LLVM to verify software written in C using such symbolic execution algorithm .
<b>Federal University of Minas Gerais, Belo Horizonte, Brazil</b>	09/2007 - 04/2008
Research Assistant at Computer Engineering Laboratory	
Main Activities:	Collaborated in the development of an architecture fault tolerant employing runtime verification techniques. Implemented a MIPS based fault tolerant processor in Verilog and OVL.
<b>Federal University of Minas Gerais, Belo Horizonte, Brazil</b>	04/2008 - 09/2008
Research Assistant at Laboratory of Access Universalization	
Main Activities:	Collaborated in the development of a system to track samples from the first stage until the final step of protein identification, named PRODIS, using perl, php, MySQL.

## Main Refereed Publications

---

<b>Journal Publication</b>	Safe, G. P.; Coelho, C.; Vieira, L. F. M. ; Val, C. G.; Nacif, J. A. M.; Fernandes, A. O.; "Selection of formal verification heuristics for parallel execution," STTT, vol. 14, no. 1, pp. 95-108, 2012.
<b>Conference Publication</b>	Sam Bayless, Celina Val, Thomas Ball, Holger Hoos and Alan Hu. "Efficient Modular SAT Solving for IC3". To appear in Formal Methods in Computer-Aided Design (FMCAD), 2013.  Alex Horn, Michael Tautschnig, Celina Val, Lihao Liang, Tom Melham, Jim Grundy and Daniel Kroening. "Formal Co-Validation of Low-Level Hardware/Software Interfaces". To appear in Formal Methods in Computer-Aided Design (FMCAD), 2013.  Cardoso, T. N. C.; Val, C. G.; Nacif, J.A.; Fernandes, A.O.; Coelho Jr, C.N.. "Assertion based fault-tolerant processor: How to recover from design errors." IFIP International Conference on Very Large Scale Integration and System-on-Chip, 2008, Rhodes.

## Other Interests

---

Music, Snowboard, Soccer, Dancing, Traveling